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(54) Title: PROCESS FOR FORMING A CMOS INTEGRATED CIRCUIT STRUCTURE
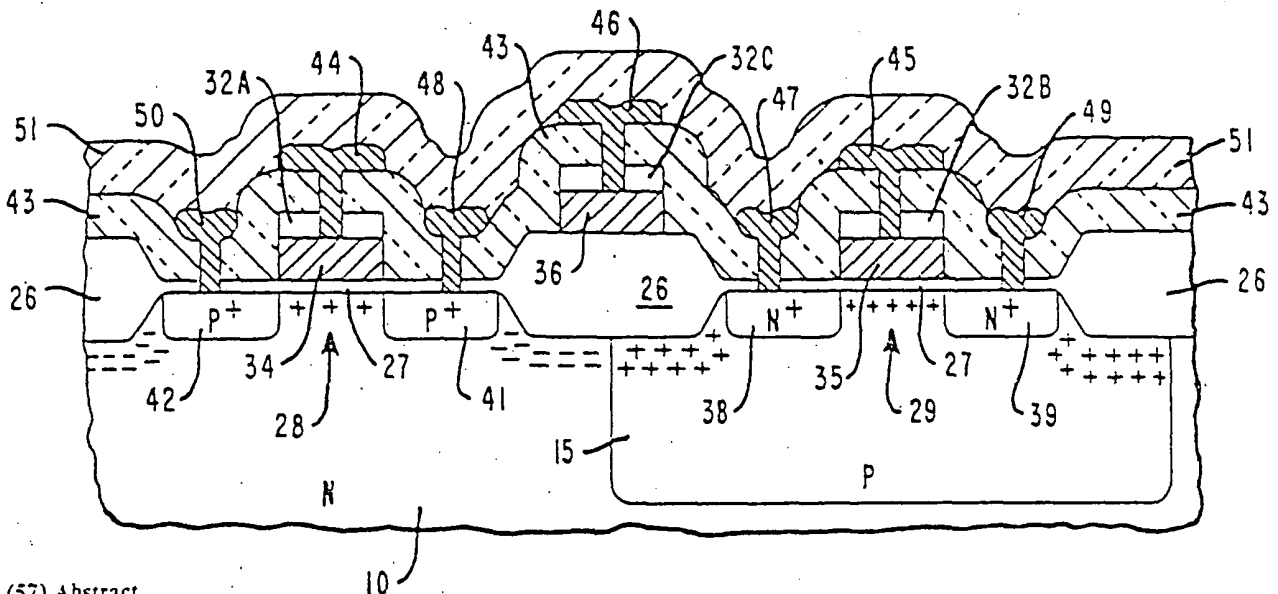
(57) Abstract

In a process for forming a complementary semiconductor device in a semiconductor substrate having first and second active regions therein a thin gate oxide layer (27) is formed on the substrate (10) and a polysilicon layer (31) is formed on the gate oxide layer (27). The polysilicon layer (31) is then doped to the desired level with n-type impurities, whereafter a relatively thick mask oxide layer (32) is formed on the polysilicon layer (31). Polysilicon gate electrodes (34, 35) and interconnecting conductors (36) are defined and etched from the doped polysilicon layer (31) leaving portions (32A, 32B) of the mask oxide layer remaining on the gate electrodes (34, 35). The first and second active regions are then alternately masked, while effecting ion implantation of dopants to form source and drain regions (38, 39 and 41, 42). During the ion implantation the mask portions (32A, 32B) protect the polysilicon gate electrodes (34, 35) from further doping.

PROCESS FOR FORMING A CMOS
INTEGRATED CIRCUIT STRUCTURE

Technical Field

This invention relates to processes of the
5 kind for forming an integrated circuit from a structure
including a body of a semiconductor material having a
first active region of a first conductivity type, a
second active region of the second conductivity type,
and a silicon dioxide layer formed on said body encom-
10 passing respective gate regions within said active re-
gions.

Background Art

A CMOS device consists of an n-FET and a p-FET
which are coupled so that the source or drain of one
15 device is connected to the source or drain of the other
device. In operation, one of the transistors will be
functioning and the other will be off. When operating
conditions within the circuit dictate that the func-
tioning transistor turn off, the transistor which was
20 previously off will begin to function due to the inter-
connection of sources and/or drains of the two trans-
istors. Thus, very little power is required during the
non-switching state for these transistors, thereby
enabling reduced power consumption. Other advantageous
25 features of a CMOS device include high speed and per-
formance. Balanced against these is the complexity of
the processing technology of CMOS devices, particularly
in meeting the stringent requirements of high inte-
gration (or packing) density and high performance in
30 very large scale integrated circuit applications.

In an attempt to meet the above requirements,
conventional metal gate CMOS processing techniques have
been replaced by silicon gate technology since this
provides an area savings due to the better tolerances
35 arising from the self-aligned nature of such gate

structures, due to the ability to provide an additional
layer of interconnect and due to the availability of
buried contacts.

An example of a silicon gate CMOS process,
5   International Patent Application Publication No. WO82/
02283 (European Publication No. 0067206), discloses form-
ing the desired pattern of gate electrode and intercon-
necting conductors on a semiconductor substrate such
that each of the gate electrodes and conductors overlies
10   a thin layer of gate oxide and is covered by a suitable
oxidation and diffusion mask. The oxidation and dif-
fusion mask, which consists of a dual layer of silicon
dioxide and silicon nitride, serves as an oxidation mask
and an implant/diffusion mask for the gate electrodes.
15   The source and drain regions of the p-FET's and n-FET's
are alternatively masked and formed by diffusing or im-
planting p-type and n-type impurities into the substrate.
A layer of barrier oxide is then thermally grown on the
semiconductor substrate to completely cover the source
20   and drain regions, thereby protecting these regions from
further doping during subsequent doping of the gate
electrodes and conductors. Thereafter, the oxidation
and diffusion mask which overlies each of the gate
electrodes and conductors is selectively removed (while
25   leaving the source and drain regions covered), thereby
exposing the underlying gate electrodes and conductors.
The exposed gate electrodes and conductors are then
doped using a conventional doping technique.

Using this process a CMOS device having poly-
30   silicon gates of a single conductivity and n-type im-
purities is provided.

Because all of the gate electrodes and con-
ductors have the same type of impurities, the need for
metal bridges between (n^+ and p^+) polysilicon conduc-
35   tors, which would otherwise be required, is avoided
thereby making more efficient use of chip area. Also,
because all the gate electrodes are not subjected to

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p-type dopant (e.g., boron) the problem of dopant
(particularly, boron) penetration from the gate elec-
trode, through the thin oxide layer which separates the
gate electrode from the underlying semiconductor sub-
5   strate, and into the underlying substrate thereby chan-
ging the threshold voltage of the p-FET or producing a
short between their source and drain regions is elimi-
nated.

        The process discussed above has the disadvan-
10   tage that the oxidation of source and drain regions may
consume some of the dopant in these regions. This may
result in a higher source-to-drain interconnect resis-
tance, thereby decreasing the device speed.

Disclosure of the Invention

15   It is an object of the present invention to
provide a process of the kind specified wherein the
aforementioned disadvantage is alleviated.

        Therefore, according to the present invention,
there is provided a process of the kind specified char-
20   acterized by the steps of forming, over said silicon
dioxide layer, a polysilicon layer doped to the desired
conductivity level for gate electrodes, patterning said
polysilicon layer into gate electrodes corresponding to
said first and second active regions, and forming source
25   and drain regions of a first conductivity type in said
second active region and source and drain regions of the
second conductivity type in said first active region
without further doping of said polysilicon gate elec-
trodes.

30   It will be appreciated that in a process
according to the invention the step of initially doping
to the desired level polysilicon utilized for gate
electrodes eliminates the requirement for oxidation of
the source and drain areas.

35   In brief summary of one embodiment of the
invention, first a polysilicon layer is formed over the

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p-FET and n-FET regions and then doped n^+. Thereafter, an oxide mask is formed over the n^+ polysilicon to protect the polysilicon from further doping during the n-FET/p-FET source and drain forming steps. N^+ poly-

5   silicon gates are then defined followed by forming self-aligned n-FET and p-FET source and drain regions by alternately masking and implanting n-type and p-type impurities into the substrate. Finally, without removing the oxide mask over the polysilicon gates an iso-

10   lation oxide is formed over the entire structure. Contact vias are then simultaneously etched in the different thickness oxide over the gates and source and drain regions, followed by metallization. It will be appreciated that since the mask covering the polysilicon gates

15   is not removed, the need, in the process discussed above, for precise control of the etch time for selective mask removal from the polysilicon to be doped, is eliminated.

Brief Description of the Drawings

       One embodiment of the present invention will

20   now be described by way of example with reference to the accompanying drawings, in which:

       Figs. 1-11 are cross-sectional views illustrating various process steps of the present invention for forming a CMOS device with polysilicon gates of a

25   single conductivity and single impurity type.

Best Mode for Carrying Out the Invention

       Reference is now made to Figs. 1-11 wherein the successive steps of the fabrication process of the present invention are illustrated in detail. The steps

30   to be discussed hereafter are illustrative of one technique for implementing the process of the subject invention. It will be obvious to those skilled in the microelectronics art that the specific processes for implementing the various steps may be carried out in a number

35   of different ways.

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The drawings herein are not to scale. The
scale has been changed where needed to clearly show the
structure.

Referring now to Fig. 1, the process of the
5   present invention is initiated by selecting a semicon-
ductor substrate 10 as the starting material. In order
to accommodate both p-FET's and n-FET's on one chip, it
is necessary to locate either type transistor (or both)
in an isolation well(s). In other words, n-FET's should
10   be located in p-wells formed on an n-type substrate, or
p-FET's located in n-wells formed on a p-type substrate,
or each type of transistor located in its corresponding
well formed on an n-type or p-type substrate. The
choice presented here depends on such considerations as
15   the particular application of the CMOS device, compati-
bility of this process with other processes on the
manufacturing line, and device physics, e.g., latch-up
phenomenon and transconductance of n-FET's and p-FET's.
For illustrative purposes, the substrate 10 shown in
20   Fig. 1 is n-type silicon upon which a p-well 15 is
formed. To form the p-well 15, the surface of substrate
10 is first cleaned and then oxidized, for example, by
placing in a high temperature (1,000°C.) steam oxidation
furnace, forming a relatively thick (of the order of
25   6500 Angstroms) silicon oxide 11. Next, a p-well open-
ing 12 is etched in the oxide 11 using conventional
photolithography and buffered hydrofluoric acid etching.
Then, a relatively thin (e.g., 900 Angstroms) layer of
silicon oxide 13 is thermally grown in the opening 12.
30   During this oxide 13 growing step, little or no oxida-
tion takes place in the remainder of the substrate since
the oxidation thereover is diffusion limited by the
thick oxide 11. Also, during this process step the
silicon substrate in the opening 12 is consumed to a
35   depth equal to approximately one-half of the oxide 13
thickness (i.e., 450 Angstroms, in the above example)
due to the well-accepted fact that the thickness of the

oxide grown from silicon is approximately twice that of
the silicon consumed. As a consequence of this latest
oxidation, a topographical step 14-14 (of an approximate
450 Angstroms height) is formed in the substrate, as
5   shown in Fig. 1. This topographical step will be useful
for aligning purposes at a later stage of the present
process, as explained hereinbelow.

Referring further to Fig. 1, the p-well 15 is
then formed by implanting p-type ions (such as boron)
10   into the substrate 10 through the opening 12. During
this implantation, the energy of the ions is so chosen
as to penetrate the thin oxide layer 13, but not the
thick oxide layer 11, thereby doping only the p-well 15.
For the oxide thickness specified above, typically,
15   boron ions of energy 60 keV and dose 4 x 10^{12} ions per
square centimeter is used. To achieve the proper depth
for the p-well, the structure is then subjected to a
long, high temperature diffusion cycle. An exemplary
procedure is used to introduce the structure in a fur-
20   nace having a gaseous nitrogen atmosphere at a temper-
ature of 1200°C for about 24 hours. After the comple-
tion of this step, the boron ions diffuse laterally
and downward to a distance of about 6 microns.

After forming the p-well 15, the oxide layers
25   11 and 13 are removed by using a conventional etching
technique.

Referring to Figs. 2 and 3, the next step of
the process involves formation of channel stops which
define the active region of the p-FET and n-FET to be
30   formed subsequently. Referring to Fig. 2, as a first
step in forming the channel stops, an oxide layer 16,
hereinafter called support oxide, is grown from the
substrate by dry thermal oxidation to isolate the sub-
strate 10 from the next to be formed silicon nitride
35   layer 17. The support oxide 16 prevents damage to the
silicon substrate 10 caused by stresses which would be
created on the substrate by a silicon nitride 17-silicon

10 interface. Such stresses induce dislocations in the
silicon substrate 10 which result in undesirable leakage
current channels and otherwise have a deleterious effect
on the electrical characteristics of the interface. A

5   typical thickness of the support oxide is about 550
Angstroms. Thereafter, and referring further to Fig. 2,
a pair of oxidation and implantation masks are formed over
the support oxide 16. First, nitride layer 17 is formed
on the support oxide 16, then oxide layer 18 is formed

10 on the nitride 17. The thicknesses of the nitride 17 and
oxide 18 are typically in the range of (500-600) Ang-
stroms and (1100-1300) Angstroms, respectively. The
layers 17 and 18 are then patterned in a conventional
manner using a photoresist 19 and then etched to form

15 the dual-layer masks 20 and 21 which delineate the p-FET
and n-FET active regions respectively. The topographical
steps 14-14 in the p-well 15 discussed in connection with
Fig. 1 are used to visually align the mask used to
define the photoresist 19 over the dual mask 21. As

20 shown in Fig. 3, the active regions are covered by the
masks 20 and 21, whereas the field regions are covered
only by support oxide 16.

        Referring further to Fig. 3, the channel stops
are then formed by doping the field regions which are

25 potential sites of parasitic devices. In the completely
formed CMOS device, metallized interconnect lines are
formed over the field oxide. When an exceptionally high
voltage is applied to a metallized line, the underlying
substrate is prone to be inverted causing unwanted

30 current flow between unrelated sources and drains. To
suppress such parasitic FET's the field regions are
doped, raising the threshold voltage of these regions to
a level higher than the voltage that may be applied to
the metallized lines. This field doping consists, in an

35 exemplary process, of doping the p-well field regions
22-22 with p-type impurities and the n-substrate field
regions 23-23 with n-type impurities. To dope the p-
well field regions 22-22, first, a photoresist layer 24

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is applied over the mask 20 and the n-substrate field
regions 23-23 as shown in Fig. 3.   Then, p-type ions,
such as boron, are implanted in the p-well field
regions 22-22 through the exposed support oxide 16.
5   During this implantation step, the photoresist 24 pro-
tects the n-substrate field regions 23-23 and the p-FET
active regions from doping and the mask 21 protects
the n-FET active region from doping.   The photoresist
mask 24 is then removed.

10   Next, referring to Fig. 4, the n-substrate
field regions 23-23 are doped by forming a photoresist
layer 25 over the mask 21 and the p-well field regions
22-22 and implanting with n-type ions, such as phos-
phorus, in a manner analogous to the previous step.   The
15   photoresist mask 25 is then removed.

               Referring to Fig. 5, next the field (isolation)
oxide 26 of thickness in the range 6,000-10,000 Angstroms
is grown, for example by wet oxidation at a temperature
of about 1,000°C.   During this high temperature oxida-
20   tion the nitride layer 17 of masks 20 and 21 acts as a
barrier to diffusion of oxygen species, thereby pre-
venting growth of oxide in the n-FET and p-FET active
regions.

               As shown in Fig. 6, the oxide mask 18, the
25   nitride mask 17 and the support oxide 16 are then re-
moved using conventional etching techniques.   During
this etching process, the thick field oxide regions 26
may be thinned somewhat, but not to a degree that their
dielectric function is hampered.   The bare active areas
30   are now re-oxidized to form the gate oxide 27 of thick-
ness in the range (300-1,000) Angstroms.

               It is noted that the support oxide 16 (Fig. 5)
may be left in place and used as the gate oxide.   How-
ever, a preferred procedure is to remove the oxide 16
35   (Fig. 5) and form a new oxide 27 (Fig. 6) in its place
since this procedure permits a better control of the
gate oxide thickness and also eliminates any possible

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contamination of the gate oxide which might take place
as in the case of support oxide 16 during the deposition
and subsequent etching of nitride 17, etc.

After forming the gate oxide 27, the device
5   active regions are subjected to one or two ion implan-
tations (of the same or opposite impurity type) to
adjust the threshold voltages of p-FET's and n-FET's to
the desired value. If two implantations of opposite
impurity type are used, two photoresist masks may have
10 to be used to alternately mask and implant the p-FET and
n-FET active areas. In the present exemplary process
two ion implantations of the same conductivity type are
accomplished. The type of implantation species, their
energy, and dose is a function of several factors in-
15 cluding the resistivity or doping level of the starting
material, the doping level of the p-well 15, the gate
oxide 27 thickness, the type of polysilicon gate (to be
formed later) and the actual threshold voltages desired.
For example, when the substrate 10 is n-type having a
20 $<100>$ crystal orientation and bulk resistivity of about
(3-6) ohm-centimeter, the p-well 15 sheet resistance is
about 7,000 ohms per square, the gate oxide 27 thickness
is about 600 Angstroms, the polysilicon gates (to be
formed) are n^+-type, and the desired n-FET and p-FET
25 threshold voltages are +1 volt and -1 volt, respectively,
the two implantations can be accomplished using boron
ions of different doses.

First, boron of dose 1.6×10^{11} ions per
square centimeter and energy 40 keV is implanted into
30 the entire structure. During this step, referring to
Fig. 6, the boron ions penetrate through the thin gate
oxide 27 and are lodged in the p-FET and n-FET active
regions forming the surface charge layers 28 and 29,
respectively. As a result of this implantation step,
35 the p-FET threshold voltage will be about -1 volt.

Next, referring to Fig. 7, the p-FET active
region is protected using a photoresist mask 30 and the

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exposed n-FET active area is implanted using boron ions
of a higher dose, 3.9×10^{11} ions per square centimeter,
and the same energy (of 40 keV) as before. As a result
of this second implantation, the surface charge of layer
5   29 will be increased to a level that will result if a
single implantation of dose $(1.6 \times 10^{11} + 3.9 \times 10^{11} =)$
5.5×10^{11} ions per square centimeter was used. At any
rate, this combination of implantation steps sets the n-
FET threshold voltage at about +1 volt, thereby matching
10   it with the p-FET threshold voltage. The photoresist 30
is then removed.

        Once the devices thresholds have been estab-
lished at the desired level, the polysilicon gates and
interconnecting lines can be formed. As shown in Fig. 8,
15   a polysilicon layer 31 is formed on the semiconductor
structure to a typical thickness of about 5000 Angstroms
by, for example, chemical vapor deposition at atmos-
pheric or low pressure of (0.3-1) millitorr. After
forming, the polysilicon 31 is doped heavily using, for
20   example, an n-type dopant. An exemplary process of
doping the polysilicon 31 utilizes a phosphorus pre-
deposition and furnace diffusion steps. During this
step, the back surface of the substrate 10 is also doped
for insuring good back surface ohmic contact which will
25   be beneficial during the packaging stage of the CMOS
device, and also acting as a getter for metallic impur-
ities.

        After the conductivity of the polysilicon 31
is increased to the desired level, a layer of silicon
30   oxide 32 of about 3500 Angstroms thickness is formed by
chemical vapor deposition on the polysilicon 31. The
layer 32 protects the underlying silicon 31 from addi-
tional doping during the later p-FET and n-FET source
and drain implantation steps. Then, using a photoresist
35   mask 33, the polysilicon gates and interconnecting
conductor lines are defined by sequentially etching the
oxide layer 32 and polysilicon 31 using buffered hydro-
fluoric acid and a plasma, respectively. The photoresist

33 is then removed. Two polysilicon gates 34, 35 and
one polysilicon conductor line 36 formed in the manner
just described are shown in Fig. 9. Gate 34 is for the
p-FET and gate 35 is for the n-FET. Conductor line 36

5   is formed on the top of the central field isolation
oxide 26. Note that the oxide layer 32A, 32B, and 32C
over the gates 34 and 35 and the interconnecting line
36, respectively, is not removed.

       The next step of the process, shown in Fig. 9,

10   is the formation of the source and drain for the n-FET.
An exemplary technique for forming this step of the
process involves depositing a layer of photoresist 37 on
the semiconductor structure such that it uniformly
covers the previously formed gate structures and con-

15   ductor structures, then exposing and developing the
photoresist to provide the photoresist mask 37 shown in
Fig. 9. Specifically, mask 37 covers the p-FET active
region, gate electrode 34 and conductor line 36. The
thick field oxide regions 26, regardless of whether

20   covered by mask 36 or not, of course, preserve intact
the channel stops formed thereunder. There is no need
to cover the n-FET gate electrode 35 by mask 37 because
of the presence of the oxide mask 32B. As shown, only
the active region of the n-FET is exposed. Thereafter,

25   the source 38 and drain 39 of the n-FET are formed by
implanting n-type impurities into the substrate. In
performing this implantation step, n-FET gate 35 acts as
a mask which serves to align the transistor's source 38
and drain 39 with the gate electrode 35. During this

30   implantation step, the energy of the n-type ions are so
chosen as to penetrate the thin oxide layer 27 over the
source 39 and drain 40, but do not penetrate the rela-
tively thick oxide 32B over the gate 35. Also, the n-
type ion dose is chosen sufficiently high to counterdope

35   the p-type surface layer 29 in the source 38 and drain
39 areas that was introduced previously, and produce
n^+ source 38 and drain 39. An exemplary set of implan-
tation parameters for this step is arsenic ions of dose

8×10^{15} ions per square centimeter and energy 80 keV.
The sheet resistance of the n^+ source 38 and drain 39
formed in this manner will be about 30 ohms per square.
The photoresist 37 is then removed.

5   The source and drain regions of the p-FET are
then formed in a manner analogous to the formation of
n-FET source and drain. Referring to Fig. 10, using
conventional photolithographic techniques, a photoresist
mask 40 is formed over the n-FET gate 35, source 38 and
10   drain 39, and the conductor line 36. The p-FET gate
electrode 34 is not covered by mask 40 since the oxide
layer 32A masks this electrode. Thus, only the p-FET
active region is exposed. P-type ions are then im-
planted to form the p^+ source 41 and drain 42 in a self-
15   aligned relationship with the gate 34, in a manner fully
analogous to the previous step in connection with the
formation of the n-FET source 38 and drain 39. An
exemplary set of implantation parameters to form the
source 41 and drain 42 is boron ions of dose 6×10^{15}
20   ions per square centimeter and energy 35 keV. The
photoresist 40 is then removed.

After forming the n-FET and p-FET sources and
drains, the semiconductor structure is subjected to a
high temperature anneal step to repair any damage to the
25   silicon substrate lattice that may have been caused by
the source and drain implants and to insure that the
implanted ions are electrically activated. Typically,
annealing is done at about 1000°C. in a gaseous nitrogen
atmosphere. It is noted that no specific annealing was
30   necessary after the earlier implantation steps of this
process, such as the implantations to form the channel
stops and adjust the devices threshold voltages because
during subsequent high temperature process steps, such
as oxidation steps and polysilicon 31 deposition step,
35   impurity activation naturally takes place.

The remainder of the process is well-known.
Referring to Fig. 11, which is a cross-sectional repre-
sentation of a completed CMOS device in accordance with

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the process of this invention, the remaining steps of
the process include: (1) formation of a thick (about
10,000 Angstroms) oxide 43 over the entire semiconductor
structure to serve as an electrically insulating layer;
5   (2) etching contact vias in oxide 43 corresponding to
the sources 38 and 41, drains 39 and 42, gates 34 and 35
and interconnecting conductor 36; (3) depositing a con-
ductive layer such as aluminum or aluminum-silicon alloy
over the structure; (4) delineation of this conductive
10   layer forming conductive contacts 44 and 45 for the
polysilicon gates 34 and 35, respectively, conductive
contact 46 for the interconnecting conductor 36,
conductive contacts 47 and 48 for sources 38 and 41,
respectively, contacts 49 and 50 for drains 39 and 42,
15   respectively; and (5) forming a passivation layer 51 of
a material such as phosphosilicate glass over the device.

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CLAIMS:

1.   A process for forming an integrated cir-
cuit from a structure including a body of a semicon-
ductor material (10) having a first active region of a
first conductivity type, a second active region of the
5   second conductivity type, and a silicon dioxide layer
(27) formed on said body encompassing respective gate
regions within said active regions, characterized by the
steps of forming, over said silicon dioxide layer (27),
a polysilicon layer (31) doped to the desired conduc-
10   tivity level for gate electrodes, patterning said poly-
silicon layer (31) into gate electrodes (34, 35) corres-
ponding to said first and second active regions, and
forming source and drain regions (41, 42) of a first
conductivity type in said second active region and source
15   and drain regions (38, 39) of the second conductivity
type in said first active region without further doping
of said polysilicon gate electrodes.

2.   A process according to claim 1, charac-
terized in that the step of patterning the polysilicon
layer (31) into gate electrodes (34, 35) includes the
steps of forming an oxide mask (32A, 32B, 32C) over the
5   polysilicon layer (31) defining gate electrodes therein
and etching the polysilicon layer (31) in the presence of
the oxide mask (32A, 32B, 32C) to form the gate elec-
trodes (34, 35).

3.   A process according to claim 2, charac-
terized in that the step of forming the source and drain
regions (38, 39, 41, 42) in said active regions includes
the steps of doping the substrate (10) in the presence
5   of the oxide mask (32A, 32B, 32C) to form source and
drain regions (38, 39, 41, 42) in said first and second
active regions such that said source and drain regions
(38, 39, 41, 42) are aligned with their corresponding
gate electrodes (34, 35).

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4.   A process according to claim 4, charac-
terized in that said oxide mask (32A, 32B, 32C) addition-
ally defines regions for interconnecting conductor (36)
in said polysilicon layer (31).

5.   A process according to claim 3, charac-
terized in that said step of forming said source and
drain regions (38, 39, 41, 42) includes the steps of
forming a first mask (37) over the second active region,

5   implanting impurities of said second conductivity type
in the source and drain regions (38, 39) in the first
active region utilizing said oxide mask (32A, 32B, 32C)
as an implantation mask, removing said first mask (37),
forming a second mask (40) over said first active region,

10   and implanting impurities of said first conductivity
type in the source and drain regions (41, 42) in the
second active region utilizing said oxide mask (32A,
32B, 32C) as an implantation mask.

6.   A process according to claim 5, charac-
terized in that said first and second masks (37, 40) are
of photoresist material.

7.   A process according to claim 1, charac-
terized in that said step of forming said polysilicon
layer (31) includes the steps of depositing polysilicon
to a desired thickness and doping the deposited poly-

5   silicon with n-type impurities.

8.   A process according to claim 7, charac-
terized in that the deposited polysilicon is doped with
phosphorus.

9.   A process according to any one of the pre-
ceding claims, characterized in that the thickness of
said silicon dioxide layer (27) is in the range of 300-
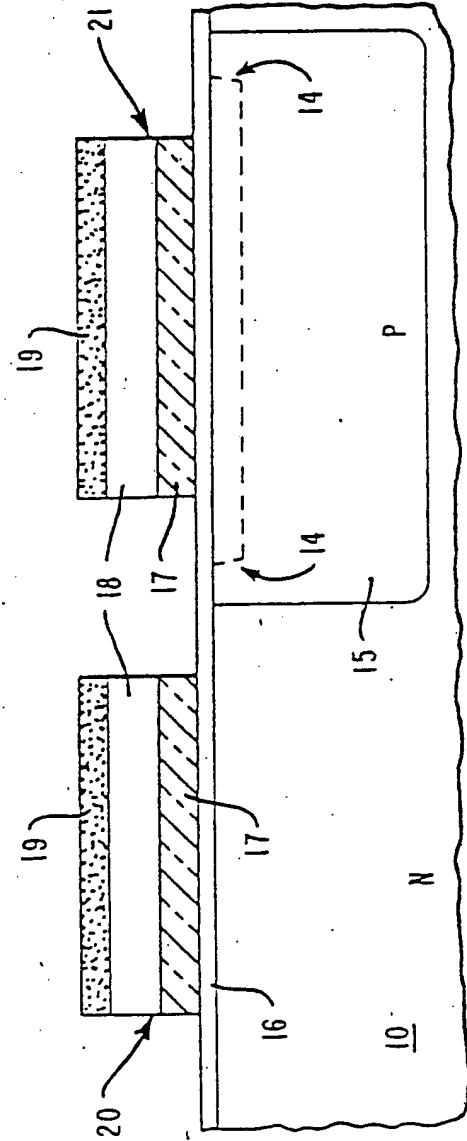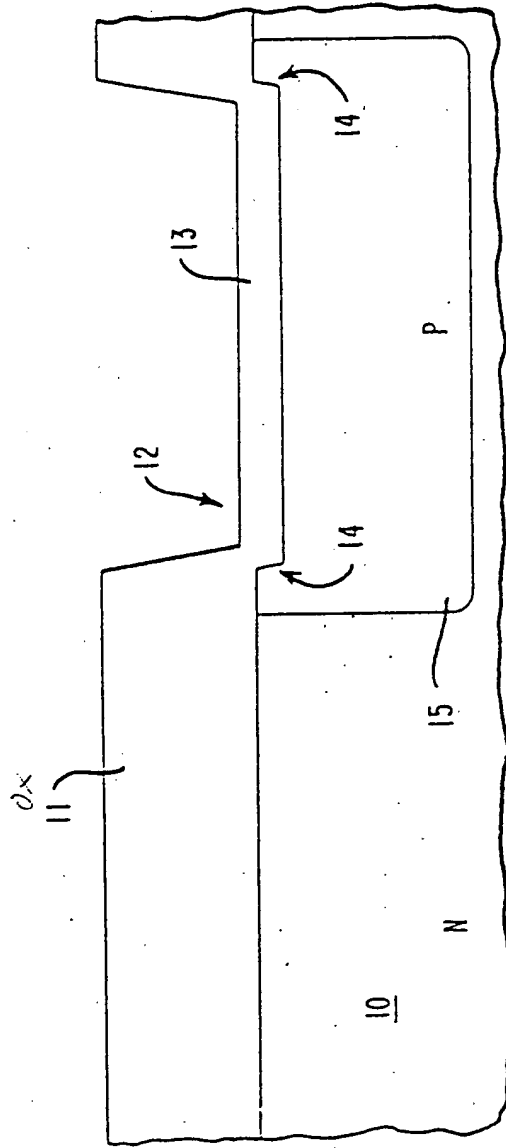100 Angstroms, the thickness of said polysilicon layer

9. (concluded)

5   (31) is about 5000 Angstroms and the thickness of said
     oxide mask layer (32A, 32B, 32C) is about 3500 Angstroms.

INTERNATIONAL SEARCH REPORT

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[3]: H 01 L 21/82; H 01 L 21/28; H 01 L 29/62

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC[3]	H 01 L

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched [6]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category [*]	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US, A, 3999213 (U.S. PHILIPS CORP.) 21 December 1976, see column 9, line 31 - column 10, line 4; figures 8-11	1-8
Y	US, A, 4033797 (HUGHES AIRCRAFT CO.) 5 July 1977, see column 7, line 45 - column 8, line 50; figures 7e-7h	1,3-7
Y	US, A, 4295897 (TEXAS INSTRUMENTS) 20 October 1981, see column 2, line 66 - column 3, line 25; figures 6,7	1,3-8

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

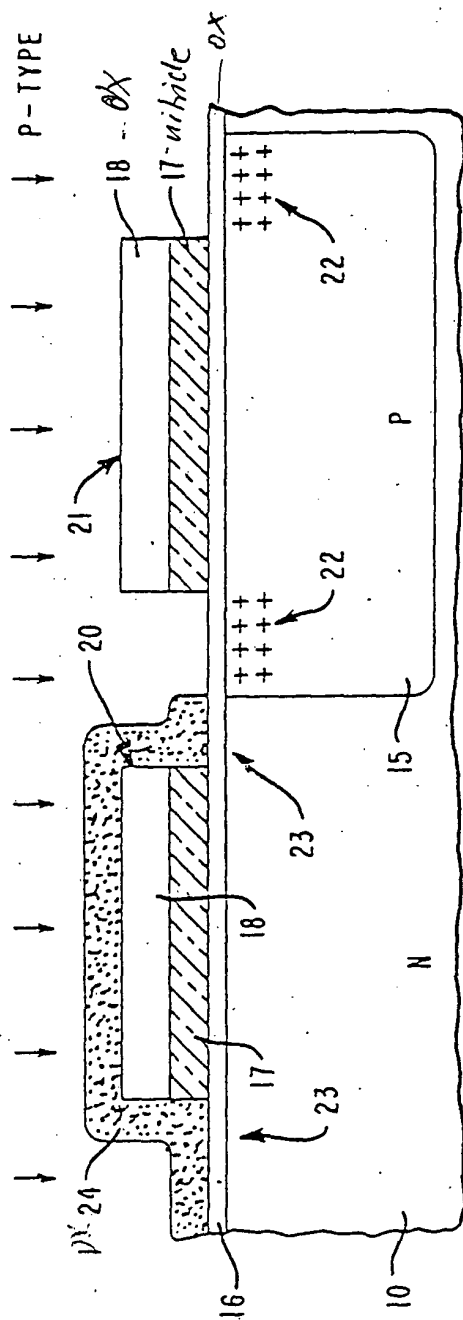| Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
22nd April 1983	1 1 MAI 1983
International Searching Authority [1]	Signature of Authorized Officer [20]
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

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FIG.1

FIG.2

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FIG. 3

FIG. 4

FIG.5

FIG.6

FIG.7

FIG.8

FIG. 9

FIG. 10

FIG.11